FORM PTO-1449

SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.
1778.0180000

FIRST NAMED INVENTOR
Christopher R. Risucci
FILING DATE
August 10, 2001

Page 1 of 3

APPLICATION NO.
09/925,314

O PE
ART UNIT
2183

JUN 3 0 2005

EXAMINER			U.S. PAT	ENT DOCUMENTS		12	A S
		DOCUMENT				SUB-	RANGERIA
NITIAL .		NUMBER	DATE	NAME	CLASS	CLASS	PILING DATE
•	AA1	3,794,980	02/1974	Cogar et al.			
	AB1	3,811,114	05/1974	Lemay et al.		1	
	AC1	3,840,861	10/1974	Amdahl et al.		1	<u> </u>
	AD1	3,983,541	09/1976	Faber et al.			
	AE1	4,110,822	08/1978	Porter et al.			
	AF1	4,149,244	04/1979	Anderson et al.		ļ	
	AG1	4,229,790	10/1980	Gilliland et al.			
	AH1	4,295,193	10/1981	Pomerene, James H.			
7	Al1	4,432,056	02/1984	Aimura, Harutsugu			
7	AJ1	4,467,409	08/1984	Potash et al.			
	<u> </u>		FOREIGN P	ATENT DOCUMENTS		•	
EXAMINER NITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
47	AK1	EP 0 073 424 A2	03/1983	Europe			N/A
1	AL1	EP 0 239 081 B1	09/1995	Europe			N/A
15	AM1	EP 0 368 332 B1	09/1997	Europe	<u> </u>		N/A
	.1	OTHER (Incl	uding Autho	r, Title, Date, Pertinent Pa	ages, etc.)		-
11 _	1	1					
45	AN1	Cobb, Paul, "TinyRIS 13 slides (7 pages) (6 embedded CPU core," Pr 3, 1996).	esentation (for Micropro	ocessor Forum,
	AN1	13 slides (7 pages) (October 22-23				
45		U.S. Utility Patent Ap (not published) (67 p	optication No. ages).	3, 1996).	sen, M., <i>et a</i>	al., filed Oct	ober 30, 2000
1	AO1	U.S. Utility Patent Ap (not published) (67 published) (71 published) (71 published) (71 published) (71 published)	optication No. ages). Application No. ages).	3, 1996). 09/702,112, inventors Jens	sen, M., et a	al., filed Oct	ober 30, 2000 ober 30, 2000
45	AO1	U.S. Utility Patent Ap (not published) (67 p U.S. Utility Patent Ap (not published) (71 p U.S. Reissue Patent 2002 (based on U.S.	plication No. ages). pplication No. ages). Application No. Application No. 6,02 ent, filed Febes Nevill, filed	3, 1996). 09/702,112, inventors Jens 09/702,115, inventors Jens 10. 10/066,475, inventor Ed	sen, M., et a sen, M., et a ward Colles 2000) (9 pa	al., filed Oct al., filed Oct s Nevill, filed ges).	ober 30, 2000 ober 30, 2000 d February 1,
TAMINER EXAMINER	AO1	U.S. Utility Patent Ap (not published) (67 p U.S. Utility Patent Ap (not published) (71 p U.S. Reissue Patent 2002 (based on U.S. Preliminary Amendm inventor Edward Coll	plication No. ages). pplication No. ages). Application No. Application No. 6,02 ent, filed Febes Nevill, filed	09/702,112, inventors Jens 09/702,115, inventors Jens 09/702,115, inventors Jens 10. 10/066,475, inventor Ed 21,265, issued February 1,	sen, M., et a sen, M., et a ward Colles 2000) (9 pa sue Patent a on U.S. Pat	al., filed Oct al., filed Oct s Nevill, filed ges).	ober 30, 2000 ober 30, 2000 d February 1, No. 10/066,475, ,265, issued

	TPE			
	70 ~ 3		Page 2	of 3
	S.	ATTY, DOCKET NO.	APPLICATION NO.	
FORM PTO-1449	IIIN 3 0 2005 G	1778.0180000	09/925,314	
, 5,	JUH 3 0 ZUGG G	FIRST NAMED INVENTOR		
SECOND SUPPLEMEN	bar. ⊠	Christopher R. Risucci		
INFORMATION DISCLOSURE S	TO SEMENT	FILING DATE	ART UNIT	
IN ONWATION BIOGEOGRAE	TRADEWENT TRADEWENT	August 10, 2001	2183	

U.S. PATENT DOCUMENTS								
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE	
12	AA2	4,507,728	03/1985	Sakamoto et al.				
1/	AB2	4,685,080	08/1987	Rhodes, Jr. et al.				
	AC2	4,724,517	02/1988	May, Michael D.				
	AD2	4,777,594	10/1988	Jones et al.				
	AE2	4,782,441	11/1988	Inagami et al.				
	AF2	5,132,898	07/1992	Sakamura et al.				
•	AG2	5,241,636	08/1993	Kohn, Leslie D.				
	AH2	5,327,566	07/1994	Forsyth, Mark A.				
	Al2	5,355,460	10/1994	Eickemeyer et al.				
125	AJ2	5,506,974	04/1996	Church et al.				
			FOREIGN P	ATENT DOCUMENTS				
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION	
12-5)	AK2	EP 0 449 661 B1	11/1995	Europe			N/A	
	AL2						Yes No	
/	AM2						Yes No	
OTHER (Including Author, Title, Date, Pertinent Pages, etc.)								
1257	AN2	Gwennap, Linley, "VLIW: The Wave of the Future?: Processor Design Style Could Be Faster, Cheaper Than RISC," <i>Microprocessor Report</i> , Vol. 8, No. 2, pp. 18-21 (February 14, 1994).						
	AO2	Kurosawa, K., et al., "Instruction Architecture For A High Performance Integrated Prolog Processor IPP," Logic Programming: Proceedings of the Fifth International Conference and Symposium (August 15-19, 1988), MIT Press, Cambridge, MA, Vol. 2, pp. 1506-1530 (1988).						
	IBM Technical Disclosure Bulletin, "Patchable Read-Only Storage and Other Patchable Functions," Vol. 27, Issue 6, pp. 3496-3499 (November 1, 1984) (4 pages).							
	AQ2	IBM Technical Disclosure Bulletin, "Patch RAM Load Technique," Vol. 27, Issue 6, pp. 3597-3598 (November 1, 1984) (3 pages).						
12	IBM Technical Disclosure Bulletin, "Microcode Memory Changes," Vol. 21, Issue 1, pp. 341-342 (June 1, 1978) (3 pages).							
EXAMINER		Veny		•	DATE C	ONSIDERED	101-	
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.								

FORM PTO-1449

SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

and not considered. Include copy of this form with next communication to Applicant.

ATTY. DOCKET NO.

1778.0180000

FIRST NAMED INVENTOR
Christopher R. Risucci
FILING DATE

APPLICATION NO
09/925,314

ART UNIT

August 10, 2001

JUN 3 0 2005

2183

Page 3 of 3

U.S. PATENT DOCUMENTS DOCUMENT SUB-**EXAMINER** CLASS **FILING DATE CLASS** INITIAL NUMBER DATE NAME AA3 5,574,873 11/1996 Davidian, Gary G. 03/1998 AB3 Vassiliadis et al. 5,732,234 AC3 6,266,765 B1 07/2001 Horst, Robert W. AD3 08/2001 Kawasaki et al. 6,272,620 B1 09/2001 AE3 2001/0021970 A1 Hotta et al. 2004/0054872 A1 03/2004 AF3 Nguyen et al. AG3 AH3 AI3 AJ3 **FOREIGN PATENT DOCUMENTS** EXAMINER DOCUMENT SUB-CLASS NUMBER **TRANSLATION** INITIAL DATE COUNTRY **CLASS** Yes AK3 No Yes AL3 No Yes AM3 No OTHER (Including Author, Title, Date, Pertinent Pages, etc.) NEC Data Sheet, MOS Integrated Circuit, uPD30121, VR4121 64-/32-Bit Microprocessor (Copyright AN3 NEC Electronics Corporation 2000) (76 pages). Ross, Roger, "There's no risk in the future for RISC," Computer Design, Vol. 28, No. 22, pp. 73-75 AO3 (November 13, 1989). NEC User's Manual, VR4100 Series[™], 64-/32-Bit Microprocessor Architecture, pp. 1-11 and 54-83 AP3 (Chapter 3) (Copyright NEC Corporation 2002). AQ3 AR3 **EXAMINER** DATE CONSIDERED 0 EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance

Page 1 of 1

FORM PTO-1449

THIRD SUPPLEMENTAL Christopher R. Risucci

INFORMATION DISCLOSURE STATE FALLER

ATTY. DOCKET NO.

APPLICATION NO.

09/925,314

FIRST NAMED INVENTOR

Christopher R. Risucci

FILING DATE

August 10, 2001

ART UNIT

2183

.

U.S. PATENT DOCUMENTS									
EXAMINER INITIAL	_	DOCUMENT	DATE	NAME	CLASS	SUB- CLASS	FILING DATE		
INITIAL	AA1	NUMBER	DATE	INAIVIC	CLASS	CLASS	FILING DATE		
				<u> </u>		1			
	AB1					<u> </u>			
	AC1					<u> </u>			
<u>,</u>	AD1								
	AE1					ļ			
<u>-</u> .	AF1								
	AG1								
	AH1								
	Al1								
	AJ1					1			
	AK1								
	L	<u> </u>	FOREIGN	PATENT DOCUMENTS	<u></u>	<u>. L</u>			
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION		
INITIAL	AL1	NOWBER	DATE	COUNTRY	CLASS	CLASS	Yes		
•							No Yes		
	AM1						No		
	AN1						Yes No		
	AO1						Yes No		
	AP1						Yes No		
	L	OTHER (Inc	luding Auth	or, Title, Date, Pertiner	nt Pages, etc.)				
Case, Brian, "ARM Architecture Offers High Code Density: Non-Traditional RISC Encodes Many Options in Each Instruction," <i>Microprocessor Report</i> , Vol. 5, No. 23, pgs. 11-14 (December 18, 1991).									
	AS1								
	AT1	, 1	7.						
EXAMINER		/ Of m	Ju	•	DATE	ONSIDERE	08/12/00		
EXAMINER: Ini	tial if refe	rence considered, whether	r or not citation i	s in conformance with MPEP 6	609. Draw line thro	ugh citation if	not in conformance		
and not conside	red. Inch	and not considered. Include copy of this form with next communication to Applicant.							